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Appl. No. 10/799,316

Amdt. dated March 18, 2008

Reply to Office Action of November 23, 2007

Remarks

The present amendment responds to the Official Action dated November 23, 2007. A

petition for a one month extension of time and authorization to charge our credit card the one

month extension fee of \$120 accompany this amendment. The Official Action objected to the

Abstract. Claims 1-6 were rejected under 35 U.S.C. § 112 second paragraph. Claims 1-14 were

rejected under 35 U.S.C. § 101. These grounds of rejection are addressed below. Claims 1-8

have been amended to be more clear and distinct. Claims 15-19 have been canceled without

prejudice confirming a previous election. Claims 1-14 are presently pending.

Amendment to the Specification

The Official Action objected to the Abstract as containing an undefined acronym VLIW.

The Abstract has been amended to address this objection by changing "VLIW" to "very long

instruction word (VLIW)".

Section 112, Second Paragraph Rejection

The Official Action objected to the use of the terms "may be" and "combining like" in

independent claims 1 and 4. Claims 1 and 4 have been amended by changing "may be" to "is"

and "combining like" to "combining". The Section 112, second paragraph rejection should now

be withdrawn.

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Section 101 Rejection

The Official Action suggested that claims 1-14 disclose steps/elements of performing mathematical functions without disclosing a practical application with a concrete, useful, and tangible result.

Claim 1 has been amended to claim "computing the recurrence relation using the combined x^{m-i} polynomial coefficient terms in the single function GF(2^m) multiplication operation to produce a GF(2^m) result; and storing the GF(2^m) result in memory in a computer readable form". Emphasis added. Claim 4 has been amended to claim "computing the recurrence relation using the combined x^{m-i} polynomial coefficient terms in the single function GF(2^m) multiplication operation thereby calculating m by m bits for the GF(2^m) multiplication function to produce an m bit GF(2^m) result; and storing the m bit GF(2^m) result in memory in a computer readable form". Emphasis added. Claim 7 has been amended to claim "a logic device producing A XOR B XOR Y(i-1)_{j-1} as result Y(i)_j to be utilized in one or more GF multiplication circuit cells or stored in a processor accessible storage unit". Emphasis added. Claims 1, 4, and 7 as amended claim a concrete, useful, and tangible result. The Section 101 rejection of claims 1-14 should be withdrawn.

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Conclusion

As no art rejections have been made, withdrawal of the present rejection and prompt allowance are requested.

Respectfully submitted,

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